WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor substrate;

an interlayer insulating layer formed above said semiconductor substrate;

a first metal interconnection embedded in said interlayer insulating layer with a surface thereof exposed to substantially the same plane as a surface of said interlayer insulating layer;

a diffusion preventive layer formed on at least said first metal interconnection to prevent diffusion of a metal included in said first metal interconnection;

a nitrogen-doped silicon oxide layer formed on said diffusion preventive layer;

a fluorine-doped silicon oxide layer formed on said nitrogen-doped silicon oxide layer; and

a second metal interconnection embedded in said fluorine-doped silicon oxide layer with a surface thereof exposed to substantially the same plane as a surface of said fluorine-doped silicon oxide layer, and electrically connected to said first metal interconnection.

2. The semiconductor device according to claim 1, wherein a refractive index of said nitrogen-doped silicon oxide layer is 1.50 or more, and 1.55 or less.

3. The semiconductor device according to claim 1,

wherein a nitrogen concentration of said nitrogen-doped silicon oxide layer is 6 atomic % or more, and 10.5 atomic % or less.

4. The semiconductor device according to claim 1, further comprising another diffusion preventive layer formed on at least said second metal interconnection to prevent diffusion of a metal included in said second metal interconnection.

5. The semiconductor device according to claim 1, wherein said second metal interconnection comprises a plug with a predetermined width and an interconnection with a width different from said predetermined width.

6. The semiconductor device according to claim 1, wherein said interlayer insulating layer comprises a fluorine-doped silicon oxide layer.

7. A semiconductor device, comprising:

a semiconductor substrate;

an interlayer insulating layer formed above said semiconductor substrate;

a first metal interconnection embedded in said interlayer insulating layer with a surface thereof exposed to substantially the same plane as a surface of said interlayer insulating layer;

a diffusion preventive layer formed on at least said first metal interconnection to prevent diffusion of a metal included in said first metal

interconnection;

a first nitrogen-doped silicon oxide layer formed on said diffusion preventive layer;

a fluorine-doped silicon oxide layer formed on said first nitrogen-doped silicon oxide layer;

a second nitrogen-doped silicon oxide layer formed on said fluorine-doped silicon oxide layer; and

a second metal interconnection embedded in said fluorine-doped silicon oxide layer with a surface thereof exposed to substantially the same plane as a surface of said second nitrogen-doped silicon oxide layer, penetrating through said second nitrogen-doped silicon oxide layer, and electrically connected to said first metal interconnection.

8. The semiconductor device according to claim 7, wherein a refractive index of said first and said second nitrogen-doped silicon oxide layers is 1.50 or more, and 1.55 or less.

9. The semiconductor device according to claim 7, wherein a nitrogen concentration of said first and said second nitrogen-doped silicon oxide layers is 6 atomic % or more, and 10.5 atomic % or less.

10. The semiconductor device according to claim 7, further comprising another diffusion preventive layer formed on at least said second metal interconnection to prevent diffusion of a metal included in said second metal interconnection.

11. The semiconductor device according to claim 7, wherein said second metal interconnection comprises a plug with a predetermined width and an interconnection with a width different from said predetermined width.

12. The semiconductor device according to claim 7, wherein said interlayer insulating layer comprises a fluorine-doped silicon oxide layer.

13. A semiconductor device manufacturing method, comprising:

embedding an under interconnection layer in an interlayer insulating layer such that a surface thereof is exposed to substantially the same plane as a surface of said interlayer insulating layer;

forming a diffusion preventive layer to prevent diffusion of a metal included in said under interconnection layer, on at least said under interconnection layer;

forming a first nitrogen-doped silicon oxide layer on said diffusion preventive layer;

forming a fluorine-doped silicon oxide layer on said nitrogen-doped silicon oxide layer;

forming an interconnection groove and a via hole extending from a bottom of said interconnection groove above said under interconnection layer in said fluorine-doped silicon oxide layer; and

forming a plug in said via hole with a metal

layer, to be in electrically contact with said under interconnection layer, and an upper interconnection layer in said interconnection groove with said metal layer, to be electrically contact with said plug.

14. The semiconductor device manufacturing method according to claim 13, wherein said forming a first nitrogen-doped silicon oxide layer on said diffusion preventive layer includes setting a refractive index of said first nitrogen-doped silicon oxide layer to be 1.50 or more and 1.55 or less.

15. The semiconductor device manufacturing method according to claim 13, wherein said forming a first nitrogen-doped silicon oxide layer on said diffusion preventive layer includes setting a nitrogen concentration of said first nitrogen-doped silicon oxide layer to be 6 atomic % or more and 10.5 atomic % or less.

16. The semiconductor device manufacturing method according to claim 13, further comprising forming another diffusion preventive layer on at least said upper interconnection layer to prevent diffusion of a metal included in said upper interconnection layer.

17. The semiconductor device manufacturing method according to claim 13, wherein said interlayer insulating layer comprises a fluorine-doped silicon oxide layer.

18. The semiconductor device manufacturing method according to claim 13, further comprising, after said

forming a fluorine-doped silicon oxide layer on said first nitrogen-doped silicon oxide layer, forming a second nitrogen-doped silicon oxide layer on said fluorine-doped silicon oxide layer,

wherein said forming an interconnection groove in said fluorine-doped silicon oxide layer includes forming said interconnection groove to penetrate said second nitrogen-doped silicon oxide layer.

19. The semiconductor device manufacturing method according to claim 18, wherein said forming a plug in said via hole and an upper interconnection layer in said interconnection groove includes forming said metal layer on said second nitrogen-doped silicon oxide layer having said interconnection groove and said via hole, with a thickness sufficient to fill up an interior of said interconnection groove and said via hole, followed by removing said metal layer over said second nitrogen-doped silicon oxide layer.

20. The semiconductor device manufacturing method according to claim 19, wherein said forming a plug in said via hole and an upper interconnection layer in said interconnection groove further includes removing said second nitrogen-doped silicon oxide layer and said metal layer formed over said fluorine-doped silicon oxide layer, after said removing said metal layer over said second nitrogen-doped silicon oxide layer.